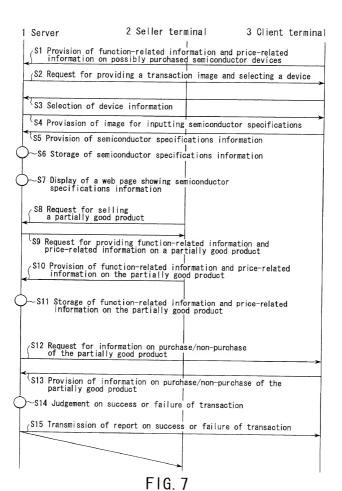


FIG. 5

<b>M</b> 2		T	Τ		T	T			T	T	T
=	T.			1	1	1	-	0	_	-   0	> -
¥		0	> <	, ,	> <		>	0	-	-   -	-
A0		,	'	1	,	,		-	-	-   -	0
ρ3	0		0	-	-   -	-  -	-	0	-	0	.   -
ρ2	0	-	-	0	C			0	-	0	-
10	-	0	-	0	-	0		0	-	0	-
φ4	0	0	-	0	-	-		1	-	0	0
φ3	0	-	0	-	0	-		0	0	-	-
φ2	-	0	0	-	-	0	,	0	0	-	-
φ	ı	-	-	0	0	0	,	-	_	0	0
Selected array	MA1 & MA2	MA1 & MA3	MA1 & MA4	MA2 & MA3	MA2 & MA4	MA3 & MA4	MA1 0 HAA	8	MA1 & MA2	MA2 & MA3	MA2 & MA3
	_	7	က	4	5	9	_			6	0

Default: AO = "1.Array MA1 & MA4 are selected AO = "0'Array MA2 & MA3 are selected

F1G. 6



Check	the device you want to buy.	
(	) DRAM	
(	) SRAM	
(	) FLASH	
ОК	~71 Cancel	~72

FIG. 8

① Degree of integration ( )M ② Access time ( )nsec ③ Operation mode ( ) ④ Desired price ( ) ⑤ Desired date of delivery ( )	② Access time ( )nsec ③ Operation mode ( ) ④ Desired price ( )				
3 Operation mode ( )  4 Desired price ( )	③ Operation mode ( ) ④ Desired price ( ) ⑤ Desired date of delivery ( )	① Degree of integration	(	) M	
Desired price     ( )	Desired price ( )     Desired date of delivery ( )	② Access time	(	)nsec	
. ,	⑤ Desired date of delivery ( )	3 Operation mode	(		)
⑤ Desired date of delivery ( )	04	① Desired price	(	)	
	OV.	⑤ Desired date of delivery	(	)	

FIG. 9

